UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/705,787	11/12/2003	Terunobu Maruyama	1602.1029	4143

21171 7590 04/21/2006

STAAS & HALSEY LLP
SUITE 700
1201 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DIMYAN, MAGID Y	
ART UNIT	**PAPER NUMBER**
2825	

DATE MAILED: 04/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/705,787	MARUYAMA ET AL.	
	Examiner	Art Unit	
	Magid Y. Dimyan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 April 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) *2-5,7-11,14-17 and 19-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,12,13 and 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/12/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of claims 1, 6, 12, 13 and 18 of Group I in the reply filed on 03 April 2006 is acknowledged. Thus, claims 1, 6, 12, 13 and 18 remain pending.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 18 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. Applicant must either store this claimed program on a computer or a computer – readable media from which they may recite the execution of the method.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claim 18 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear whether Applicants intend to claim a computer program which as stated above is clearly non – statutory, or executable method steps, in which case Applicants must amend claim language accordingly to make the claim statutory.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 6, 12, 13 and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,611,947 B1 to Higgins et al. (hereinafter, "Higgins").

7. Regarding claim 1, Higgins teaches a logical equivalence verifying device (i.e., apparatus, see Fig. 3 for performing logical equivalent verification of two prescribed circuits (see Abstract; col. 1, ll. 10 – 15) to display the results thereof (see Fig. 4, block 420), the device comprising:

(a) a first identifier section that performs structural matching in which it is determined whether there are portions in corresponding logic cones of the two circuits which correspond in circuit structure to each other (see Fig. 3, block 319; col. 10, ll. 38 – 55), and recording the result of the structure matching as an identifier for each element (see Fig. 8);

(b) a subcone extracting section for extracting a plurality of element collections as subcones (see Fig. 3, blocks 320, 330, 332; col. 10, line 56 – col. 11, line 7) from each logic cone, each element collection including elements which are connected with

each other and have the same identifier (see again Fig. 3 and 9; col. 10, line 38 – col. 11, line 7);

(c) a verifying section performing logical equivalence verification between the two circuits for each of the subcone extracted by the subcone extracting section (see Fig. 3, blocks 360 – 363; ; col. 10, ll. 56 - 63); and

(d) a display control section for displaying a first group of subcones with mismatched results of the logical equivalence verification (see Fig. 3, block 340 and Fig. 7, block 730) and a second group of subcones with matched results of the logical equivalence verification (see Fig. 7, block 720) while distinguishing between the first and second groups of subcones based on the results of the logical equivalence verification (see again Fig. 7; col. 14, line 46 – col. 15, line 12). Thus, Higgins clearly recites, or at the very least suggests, all the claimed limitations.

8. Referring to claim 13, Higgins discloses a logical equivalence verifying method for performing equivalent verification of two prescribed circuits (see Abstract; col. 1, ll. 10 – 15) to display the results thereof (see Fig. 4, block 420), the method comprising:

(a) a step for performing structural matching in which it is determined whether there are portions in corresponding logic cones of the two circuits which correspond in circuit structure to each other (see Fig. 8; col. 4, line 66 – col. 5, line 40; col. 15, ll. 13 – 20), and recording the result of the structure matching as an identifier for each element (Fig. 8);

(b) a step for extracting a plurality of element collections as subcones (see col. 6, ll. 15 – 67) from each logic cone, each element collection including elements which are

connected with each other and have the same identifier (see again Figs. 8 and 9; col. 15, ll. 13 – 44);

(c) a step for performing logical equivalence verification between the two circuits for each of the subcones (see Figs. 4, 5, 6; col. 12, line 22 – col. 13, line 20); and

(d) a step for displaying a first group of subcones with mismatched results of the logical equivalence verification (see Fig. 4, block 420 and Fig. 7, block 730) and a second group of subcones with matched results of the logical equivalence verification (see Fig. 7, block 720) while distinguishing between the first and second groups of subcones based on the results of the logical equivalence verification (see again Fig. 7; col. 14, line 46 – col. 15, line 12). Thus, Higgins clearly teaches, or at the very least suggests, all the claimed limitations.

9. As per claim 6, see Fig. 7, block 73 and col. 14, ll. 53 – 56, which teach how the results of mismatched subcones are displayed, as claimed.

10. Pursuant to claim 12, col. 2, ll. 23 – 32, which disclose the claimed limitation pertaining to the logical equivalence of a pre-change and a post-change circuit when the circuit is modified.

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 6,668,362 B1 to McIlwain et al. discloses a method and apparatus for determining equivalence between two IC device designs whereas functional blocks and

compare points within a first design are compared with functional blocks and compare points in a second design to determine compare points that are matched.

U.S. Patent No. 6,188,934 B1 to Emura teaches a register correspondence method in a logic equivalence verifying system in which input cone information is collected for each register for the two circuits to be compared.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Magid Y. Dimyan whose telephone number is (571) 272-1889. The examiner can normally be reached on Monday - Friday 8:00 AM - 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Magid Y Dimyan
Examiner
Art Unit 2825

A. M. Thompson
Primary Examiner
Technology Center 2800

myd
17 April 2006